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EXAMINER	
MERED, HABTE	
ART UNIT	**PAPER NUMBER**
2662	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,748	BEVERLY ET AL.	
	Examiner	Art Unit	
	Habte Mered	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02/22/2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 33* is/are rejected.

7)☒ Claim(s) *31,32 and 34-55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-55 are pending.

Specification

2. The abstract of the disclosure is objected to because the length of the abstract is more than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-22** are rejected under 35 U.S.C. 102(e) as being anticipated by Walker et al (US Pub. No. 2004/0228364), hereinafter referred to as Walker.

Walker discloses a coding method for coding packetized serial data with low overhead when implemented to convert a 64-bit frame to a 66-bit frame.

5. Regarding **claims 1 and 11**, Walker discloses a method and device comprising: receiving a data frame of a first size **(Figure 8B, element 310 receiving data frame of size 41 bits and last line in Paragraph 133)**; demultiplexing the data frame **(Figure 8B, elements 303 and 311)**; writing blocks of the demultiplexed data frame at the first size into a register **(Figure 8B, elements 311 and 304)**; reading blocks of a second size **(Figure 8B, elements 313 and 304)**, different from the first size **(Figure 8B,**

element 317, 64 bits), from the register **(Figure 8B, element 304)**; and multiplexing the blocks to form an output data frame of the second size **(Figure 8B, element 308 is the assembler and is shown to contain a multiplexer in Figure 1, element 34 as discussed in Paragraphs 142.) (See also Paragraphs 133 to 142 for a detailed discussion.)**

6. Regarding **claim 2**, Walker discloses a method wherein receiving a data frame of a first size includes receiving a 64-bit data frame. **(See Figure 1 – encoder 100 receiving 64 bits and see also Paragraphs 56, 130 and 131)**

7. Regarding **claims 3 and 16,** Walker discloses a method wherein demultiplexing the data frame includes providing the data frame to a one to thirty-three demultiplexer. **(See Paragraphs 36 and 38 – Walker discloses a bus narrower than 66 conductors can be used which in effect determines the size of the demux and 1:33 demux can be used in his system)**

8. Regarding **claims 4 and 18**, Walker discloses a method wherein writing blocks of the demultiplexed data frame at the first size includes writing blocks of 64-bits to a register. **(See Figure 8B element 304 – a block of 41 bits is written in the register but a block of 64-bits could have been used which is strictly dependent on the output of the demux.)**

9 Regarding **claims 5 and 19**, Walker discloses a method wherein writing the blocks into a register include writing 2,112 bits into a register. **(The register in Walkers system can potentially place store more than 2112 bits because the mux 34 in**

Figure 1 takes 66 input which means the register can store 66x41 bits= 2506 total bits at a time.)

10. Regarding **claim 6**, Walker discloses a method including controlling a write pointer at a frequency of approximately 161 MegaHertz. **(It is inherent to have some form of a pointer mechanism when using a register to store different blocks of data to keep track of what is stored where.)**

11. Regarding **claim 7**, Walker discloses a method wherein reading blocks of the second size includes reading blocks of sixty-six bits from the register. **(See Figure 1, element 100 that encodes 64-bit to 66-bit and the encoder further illustrated in Figure 8B. See Paragraph 130 and 131)**

12. Regarding **claim 8**, Walker discloses a method of including controlling a read pointer at a frequency of approximately 156 MegaHertz. **(It is inherent to have some form of a pointer mechanism when reading different blocks of data from a register to keep track of what is read and what is not read.)**

13. Regarding **claims 9 and 17,** Walker discloses a method wherein multiplexing the blocks to form an output data frame of a second size includes forming an output data frame by using a thirty-two to one multiplexer. **(See Paragraphs 36 and 38 – Walker discloses a bus narrower than 66 conductors can be used which in effect determines the size of the multiplexer and 32:1 mux can be used in his system)**

14. Regarding **claims 10 and 15**, Walker discloses a method including converting a sixty-four bit data frame to a sixty-six bit data frame. **(See Figure 1, element 100,**

encoder converting a 64-bit data frame to 66-bit data frame. See Paragraphs 52 and 56).

15. Regarding **claim 12**, Walker discloses a device of including a first counter to control the writing of data from the demultiplexer to the register. **(See Figure 8B, the output of the demultiplexer being written into the register. It is inherent for writing data in parallel to the register to have a control mechanism in the form of pointer for the purpose of keeping track what is written where and a counter is one form of implementing a pointer.)**

16. Regarding **claim 13**, Walker discloses a device including a second counter to control the reading of data from the register to the multiplexer. **(See Figure 8B, data is read from the output of the register and fed to the multiplexer. It is inherent for reading data in parallel from the register to have a control mechanism in the form of pointer for the purpose of keeping track what is read where and a counter is one form of implementing a pointer.)**

17. Regarding **claim 14**, Walker discloses a device wherein data is written to the register at approximately 161 MegaHertz and data is read from the multiplexer at approximately 156 MegaHertz. **(This is strictly a design choice and the Applicant does not provide any unique advantage for choosing such a rate. However there is nothing to prevent Walker's register from clocking in and clocking out data as such rate.)**

18. Regarding **claim 20**, Walker discloses a device wherein the demultiplexer writes data in blocks of a first size **(Figure 8B, element 311)** to the register **(Figure 8B,**

element 304) and the multiplexer **(Figure 8B, element 308 further illustrated in Figure 1, element 34)** reads data in blocks of a second size **(Figure 8B, element 313)**, different from the first size, from the register. **(See Figure 8B, element 304 and paragraph 142)**

19. Regarding **claim 21**, Walker discloses a device wherein the device is part of a physical coding sublayer. **(See Paragraph 33 and Figure 1, element 14)**

20. Regarding **claim 22,** Walker discloses a device wherein the device is part of a receiver in a fiber optic network. **(See Paragraph 49)**

21. **Claims 23-25, 27, and 33** are rejected under 35 U.S.C. 102(e) as being anticipated by Mejia (US 6, 625, 241).

Mejia discloses a data communications bit stream combiner/decombiner with a synchronizing unit.

22. Regarding **claim 23**, Mejia teaches a method comprising: receiving a stream of data **(See Figure 2, 105 A or 105 B – see also Column 7, Line 1)**; defining a window of a predetermined size within the stream **(Figure 2, 203 – see Column 6, Line 67-Column 7, Line 1)**; examining the window to determine whether at least one synchronization bit is located within the data in the window **(Figure 2, 205 – see Column 7, Lines 4-9)**; and shifting the window along the stream if a valid synchronization bit is not found in the window **(See Figure 4 and 5 – fill words are added to shift the window – see also Column 7, Lines 50-59)** .

23. Regarding **claim 24**, Mejia discloses a method including shifting the window by a predetermined number of bits and filling the opening created by shifting with a bit from a

previous cycle. **(See Figures 4 and 5 and Column 7, Lines 44-67. The fill words from the previous cycle fill the opening in the frame and the sliding window shifts to the next bits from the incoming received stream)**

24. Regarding **claim 25**, Mejia discloses a method including storing bits from each successive cycle and providing bits from previous cycles to fill openings created by shifting in subsequent cycles. **(See Figures 4 and 5 and Column 7, Lines 44-67. The fill words from the previous cycle fill the opening in the frame and the sliding window shifts to the next bits from the incoming received stream)**

25. Regarding **claim 27**, Mejia discloses method including locating a pair of synchronization bits in a 66-bit data frame. **(Mejia's system detects the start and end of a frame. See Column 7, Lines 4-9. There is no restriction on the size of the frame Mejia's system can handle.)**

26. Regarding **claim 33**, Mejia discloses a device **(Figure 2)** comprising: a first storage element to receive a stream of data **(Figure 2, 202 or 203)**; an element to define a window of a predetermined size within the stream **(Figure 2, 202 and 204 – see Column 6, Line 67-Column 7, Line 1)**; a detector to examine the window to determine whether at least one synchronization bit is located within the data in the window **(Figure 2, 205 – see Column 7, Lines 4-9)**; and a component to shift data along the stream into the window if a valid synchronization bit is not found in the window. **(See Figure 4 and 5 – fill words are added to shift the window by the re-timer circuit 208– see also Column 7, Lines 50-59)**

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. **Claim 26 and 28-30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mejia in view of Castagna et al (US 6, 400, 732), hereinafter referred to as Castagna.

29. Regarding **claim 26**, Mejia teaches all aspects of the claimed invention as set forth in the rejection of claim 23 but fails to expressly disclose a method including successively shifting the window by one bit along the stream of data until valid synchronization bits are located.

Castagna discloses a method and apparatus for determining synchronization and loss of synchronization in a high-speed multiplexed data system.

Castagna discloses a method including successively shifting the window by one bit along the stream of data until valid synchronization bits are located. **(See Column 4, Lines 60-65 and Figure 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Mejia's' apparatus to incorporate a window sliding by one bit, the motivation being Mejia discloses a sliding window in Column 7, Line 1 but fails to

disclose how fast the window can slide and Castagna discloses a scheme by which it slides by one bit at a time.

30. Regarding **claim 28**, Mejia teaches all aspects of the claimed invention as set forth in the rejection of claim 23 but fails to disclose a method including receiving a block of data of the predetermined size in a multiplexer and multiplexing the data into a register.

Castagna discloses a method including receiving a block of data of the predetermined size in a multiplexer and multiplexing the data into a register. **(See Figure 2 multiplexer circuit and a register and Figure 13 B and Column 7, Lines 5-15)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Mejia's' apparatus to incorporate a method including receiving a block of data of the predetermined size in a multiplexer and multiplexing the data into a register. The motivation being Mejia discloses a sliding window in Column 7, Line 1 and a multiplexer in Figure 7 but fails to disclose the inter-workings of the multiplexer and Castagna does that precisely in Figure 13 B.

31. Regarding **claim 29**, Mejia teaches all aspects of the claimed invention as set forth in the rejection of claim 28 but fails to disclose a method including applying two of the bits from the register to an exclusive OR gate.

Castagna discloses a method including applying two of the bits from the register to an exclusive OR gate. **(See Figure 13B and Column 7, Lines 5-15)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Mejia's' apparatus to incorporate a method including receiving a block of data of the predetermined size in a multiplexer and multiplexing the data into a register including applying two of the bits from the register to an exclusive OR gate. The motivation being Mejia discloses a sliding window in Column 7, Line 1 and a multiplexer in Figure 7 but fails to disclose the inter-workings of the multiplexer and Castagna does that precisely in Figure 13 B.

32. Regarding **claim 30**, Mejia teaches all aspects of the claimed invention as set forth in the rejection of claim 23 but fails to disclose a method providing 66-bit blocks in successively shifted sets, each block shifted one-bit relative to the other block to a multiplexer and successively applying the 66-bit blocks to a register.

Castagna discloses a method providing 66-bit blocks **(Castagna's system is not dependent on the size of the frame and can handle 66 bit frame)** in successively shifted sets **(See Figure 5 and Column 4, Lines 47-54)**, each block shifted one-bit relative to the other block to a multiplexer and successively applying the 66-bit blocks to a register **(See Figure 2 and Figure 13B and Column 7, Lines 5-15)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Mejia's' apparatus to incorporate a method including receiving a block of data of the predetermined size in a multiplexer and multiplexing the data into a register. The motivation being Mejia discloses a sliding window in Column 7, Line 1 and a multiplexer in Figure 7 but fails to disclose the inter-workings of the multiplexer and Castagna does that precisely in Figure 13 B.

Allowable Subject Matter

33. **Claims 31, 32 and 34-55** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

34. **Claim 31** is allowable over the prior art of record since the cited references, taken individually or in combination fail to particularly disclose the combination of a method comprising: receiving a stream of data; defining a window of a predetermined size within the stream; examining the window to determine whether at least one synchronization bit is located within the data in the window; and shifting the window along the stream if a valid synchronization bit is not found in the window including providing serial data to a first array of multiplexers arranged in rows and columns, wherein each row corresponds to a different window position along the stream of data. It is noted that the closest prior art, Mejia, discloses a method and device of receiving a stream of data, defining a sliding window of predetermined size and detecting a synchronization pattern.

35. **Claim 34** is allowable over the prior art of record since the cited references, taken individually or in combination fail to particularly disclose the combination of a device comprising: a first storage element to receive a stream of data; an element to define a window of a predetermined size within the stream; a detector to examine the window to determine whether at least one synchronization bit is located within the data in the window; and a component to shift data along the stream into the window if a valid synchronization bit is not found in the window further including a multiplexer coupled to

the data stream and the first storage element to receive data; a second storage element coupled to the output of the multiplexer to receive a data frame; a gate coupled to the second storage element to test for the presence of at least one synchronization bit in the data frame in the second storage element; and a control to determine whether or not valid synchronization bits have been located in a series of data frames. It is noted that the closest prior art, Mejia, discloses a method and device with first storage to receive a stream of data, a means to define a sliding window of predetermined size, a component to shift data along the stream and a detector for detecting a synchronization pattern.

36. **Claim 44** is allowable over the prior art of record since the cited references, taken individually or in combination fail to particularly disclose the combination of a device comprising: a first storage element to receive a stream of data; an element to define a window of a predetermined size within the stream; a detector to examine the window to determine whether at least one synchronization bit is located within the data in the window; and a component to shift data along the stream into the window if a valid synchronization bit is not found in the window and where the first storage element includes an array of multiplexers arranged in rows and columns. It is noted that the closest prior art, Mejia, discloses a method and device with first storage to receive a stream of data, a means to define a sliding window of predetermined size, a component to shift data along the stream and a detector for detecting a synchronization pattern.

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HM
12-11-2005

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